IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a continuation of application Serial No. 10/085,182, filed February 27, 2002, ~~pending,~~ now U.S. Patent 6,693,366, issued February 17, 2004, which is a continuation of application Serial No. 09/652,208, filed August 31, 2000, now U.S. Patent 6,518,198, issued February 11, 2003.

Please amend paragraph number **[0009]** as follows:

[0009] It has been found that the incorporation of small amounts of beryllium in platinum films retards oxygen diffusion by influencing the grain structure of the platinum film. (*See*, Roland Stumpf, et al., *Retardation of O Diffusion Through Polycrystalline Pt by Be Doping,* The American Physical Society, June 15, 1999, at ~~16,047-16,052~~ 16,047-16,052 (hereinafter "Stumpf")). The platinum film was formed by sputtering, then implanted with beryllium. The use of sputtering to form platinum layers is, however, somewhat undesirable since sputtering may result in layers that do not conformally cover high aspect ratio features, such as the high aspect ratio bottom electrodes that are often present in state of the art, relatively large surface area capacitor structures.

Please amend paragraph number **[0010]** as follows:

[0010] The use of boron-doped platinum films in capacitor structures has also been investigated, but boron doping of platinum was determined not to have as significant an affect on oxygen diffusion as beryllium doping of platinum. ~~*Id.*~~ Stumpf at 16,050-51.

Please amend paragraph number **[0027]** as follows:

[0027] In an exemplary embodiment of the present invention, electroless plating techniques are employed to form a doped metal oxidation barrier. With reference to FIG. 1, a semiconductor device structure 10 is dipped into, or at least partially immersed in, an electroless plating bath 20, which forms an oxidation barrier layer 12 (see ~~FIGs. 2-4)~~ FIG. 2) on a surface of

semiconductor device structure 10. Preferably, only an active surface 11 of semiconductor device structure 10 is dipped into electroless plating bath 20. As shown, semiconductor device structure 10 is contained on a wafer. Alternatively, semiconductor device structure 10 may be included on any other known type of large scale substrate, such as a whole or partial wafer of silicon, gallium arsenide, or indium phosphide, or a silicon on insulator (SOI) type substrate, such as a silicon on glass (SOG), silicon on ceramic (SOC), or silicon on sapphire (SOS) substrate. Individual semiconductor ~~devices~~ device structures 10 or collections of individual semiconductor ~~devices~~ device structures 10 may also be plated in accordance with teachings of the present invention.

Please amend paragraph number **[0029]** as follows:

[0029] As an example, ~~an oxidation~~ oxidation barrier ~~layer~~ layers 12, 12', 12" (FIGs. 2-4) including a boron-doped noble metal (e.g., platinum, rhodium, iridium, ruthenium, palladium, or alloys including noble metals) may be formed ~~upon a~~ upon semiconductor device ~~structure~~ structures 10, 10', 10" by electroless plating techniques, in accordance with teachings of the present invention. Exemplary reducing agents for the noble metal salt include, but are not limited to, borohydride (BH_4^-) (e.g., potassium borohydride), which react with the salt of a noble metal in a way that causes a formed layer of the noble metal to be doped with boron. Of course, reducing agents that result in the introduction of other dopants into a metal layer during electroless deposition thereof are also within the scope of the present invention. A metal layer formed in accordance with teachings of the present invention may include any amount of dopant that permits the metal layer to substantially retain its electrical properties, while enhancing the ability of the metal layer to prevent oxidants from permeating same or from passing therethrough. For example, when boron is employed as a dopant in a noble metal layer, the boron may comprise about 0.1% to about 5.0% of the weight of the metal layer.

Please amend paragraph number **[0031]** as follows:

[0031] An electroless plating bath for depositing boron-doped platinum may include 10 g/L $Na_2Pt(OH)_6$, 5 g/L NaOH, 10 g/L ethylamine, and 1 g/L hydrazine, as disclosed in G.O. Mallory~~, GO~~ and ~~Hadju, J,~~ J.B. Hajdu, eds., *Electroless Plating: Fundamentals and Applications*, 432-433 (hereinafter "Mallory"). It is believed that a borohydride could be substituted for or used along with hydrazine as a reducing agent to effect deposition of a doped metal layer in accordance with teachings of the present invention. Deposition may be effected at a temperature of about 35° C. *Id.* The boron-doped platinum is plated onto a substrate, such as a semiconductor device structure, at a rate of approximately 12.7 μm/hour. *Id.* Accordingly, when the method of EXAMPLE 1 is employed, substantially conformal conductive layers having thicknesses of about 100 Å or less may be formed on semiconductor device structures, for example, as oxidation barriers for capacitor structures or as bottom electrodes for capacitor structures, in less than about one hour. Thicker layers, for example, layers having thicknesses of up to about 500 Å or more, may also be formed relatively quickly.

Please amend paragraph number **[0032]** as follows:

[0032] In an alternative embodiment of the method of the present invention, an electroless plating bath may be prepared by dissolving a substantially pure platinum sponge in aqua regia, evaporating the solution with low heat, dissolving the residue in about 4% by volume hydrochloric acid (HCl), evaporating the solution, and re-dissolving the residue in a volume of about 4% HCl at a volume of about 100 mL per gram of platinum, as disclosed in Mallory. As is also disclosed in Mallory, the resulting solution is mixed with an equal volume of about 1% hydrazine. It is believed that a borohydride could be used in place ~~of~~ of, or along ~~with~~ with, the hydrazine to effect the formation of a doped metal oxidation barrier in accordance with the present invention. Following preparation of the plating bath, the plating bath is preferably warmed from about room temperature to a temperature of about 60° C to about 70° C. A semiconductor device structure upon which a doped metal oxidation barrier layer is to be formed

is disposed in the bath for the appropriate amount of time, which, of course, depends upon the desired thickness of the doped metal layer.

Please amend paragraph number **[0042]** as follows:

[0042] Following the fabrication of oxidation barrier layer 12, bottom electrode 14, and dielectric layer ~~16 and~~ 16, other features of semiconductor device structure 10 that overlie dielectric layer 16, such as the upper electrode of capacitor 30, may be fabricated, as known in the art.